AMENDMENTS TO THE CLAIMS

1. (Currently amended) A semiconductor package comprising:

a semiconductor die having a pad-mounting surface, and a plurality of spaced apart bonding pads formed on said pad-mounting surface;

a plurality of conductive bodies, each of which has a trace part that is formed on said pad-mounting surface and that is offset from a respective one of said bonding pads in a lateral direction relative to said pad-mounting surface, and a pad-connecting part that extends from said trace part to connect electrically with the respective one of said bonding pads;

a dielectric protective layer formed on said pad-mounting surface and said conductive bodies and formed with a plurality of bump-through-holes, each of which exposes a portion of said trace part of a respective one of said conductive bodies; [[and]]

a plurality of solder bumps, each of which fills a respective one of said bump-through-holes to connect electrically with said portion of said trace part of a respective one of said conductive bodies and each of which protrudes outwardly from said protective layer; and

a pair of opposite dielectric partition walls that are formed on said pad-mounting surface at two opposite sides of each of said bonding pads, said trace part of each of said conductive bodies extending through a respective one of said partition walls in a transverse direction relative to said partition walls in such a manner that said pad-connecting part of each of said conductive bodies is disposed between said partition walls.

2. (Original) The semiconductor package of Claim 1, further comprising a plurality of metal plating layers, each of which is formed on a respective one of said bonding pads, said pad-connecting part of each of said conductive bodies being formed on a respective one of said metal plating layers.

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CHRISTENSEN O'CONNOR JOHNSON KINDNESS PLLC
1420 Fifth Avenue
Suite 2800
Seattle, Washington 98101
206.682.8100

3. (Original) The semiconductor package of Claim 1, wherein each of said conductive bodies is made from conductive paste.

4. (Original) The semiconductor package of Claim 1, wherein said protective layer is made from epoxy resin.

5. (Original) The semiconductor package of Claim 1, wherein said trace part of each of said conductive bodies includes a metal layer that is electrically connected to a respective one of said solder bumps.

6. (Original) The semiconductor package of Claim 5, wherein said metal layer includes a nickel sub-layer and a gold sub-layer.

7. (Canceled)

8. (Currently amended) The semiconductor package of Claim 1 [[7]], wherein said partition walls define an inner space therebetween, said semiconductor package further comprising an encapsulant that fills said inner space so as to cover said bonding pads.

9. (Original) The semiconductor package of Claim 8, wherein said encapsulant is made from epoxy resin.

10. (Original) The semiconductor package of Claim 8, wherein said encapsulant is made from photo-sensitive ink.

11. (Original) The semiconductor package of Claim 8, wherein said encapsulant is made from polyimide.

12. (Original) The semiconductor package of Claim 8, wherein said partition walls have a height, which is measured from said pad-mounting surface, higher than that of said trace parts of said conductive bodies, said pad-connecting parts of said conductive bodies being covered by said encapsulant.

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CHRISTENSEN O'CONNOR JOHNSON KINDNESS PLLC
1420 Fifth Avenue
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Seattle, Washington 98101
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13. (Original) The semiconductor package of Claim 8, wherein said partition walls have a height, which is measured from said pad-mounting surface, substantially equal to that of said trace parts of said conductive bodies, said pad-connecting parts of said conductive bodies being exposed from said encapsulant.

14. (Original) The semiconductor package of Claim 1, further comprising a plurality of metal plating layers, each of which is formed on a respective one of said bonding pads, and a plurality of connection-enhancing bosses, each of which is formed on and protrudes from a respective one of said bonding pads, said pad-connecting part of each of said conductive bodies being formed on a respective one of said metal plating layers and enclosing a respective one of said connection-enhancing bosses.

15. (Original) The semiconductor package of Claim 14, wherein each of said connection-enhancing bosses is made from a photoresist material.

16-49. (Canceled)

LAW OFFICES OF
CHRISTENSEN O'CONNOR JOHNSON KINDNESS PLLC
1420 Fifth Avenue
Suite 2800
Seattle, Washington 98101
206.682.8100